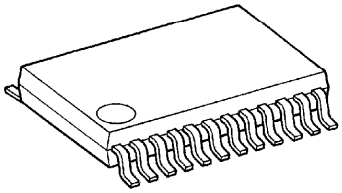
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9434AFN

Σ-Δ MODULATION DA CONVERTER WITH BUILT-IN 8-TIMES OVERSAMPLING DIGITAL FILTER / DIGITAL BASS BOOST / ANALOG FILTER

The TC9434AFN is second-order Σ-Δ modulation system 1-bit DA converters incorporating an 8-times oversampling digital filter, an analog filter and digital bass boost function developed for digital audio equipment.

Because the IC includes an analog filter, it can output a direct analog waveform, thus reducing the size and cost of the DA converter.



SSOP24-P-300-0.65A

Weight : 0.14g (Typ.)

FEATURES

- Built-in 8-times oversampling digital filter.
- Low-voltage operations (2.7V) possible.
- Built-in digital de-emphasis filter.
- In serial control mode, output amplitude can be set in 128 steps of resolution using microcontroller commands.
- In parallel control mode, soft mute can be set for the output signal in 64 steps in 20ms.
- Built-in LR common digital zero detection output circuit.
- DAC converter oversampling ratio (OSR) : 192fs.
- Two types of built-in digital bass boost function.
- Sampling frequency : 44.1kHz.
- Built-in third-order analog filter.
- The digital filter and DA converter characteristics are shown on the next page.

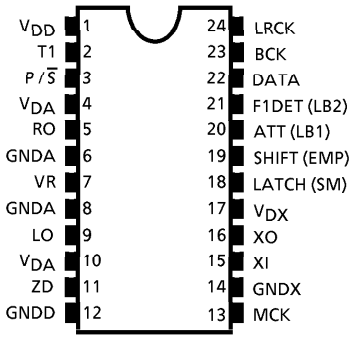
DIGITAL FILTER

	DIGITAL FILTER	PASSBAND RIPPLE	TRANSIENT BANDWIDTH	ATTENUATION
Standard Operation	8fs	±0.11dB	20k~24.1kHz	−26dB or less

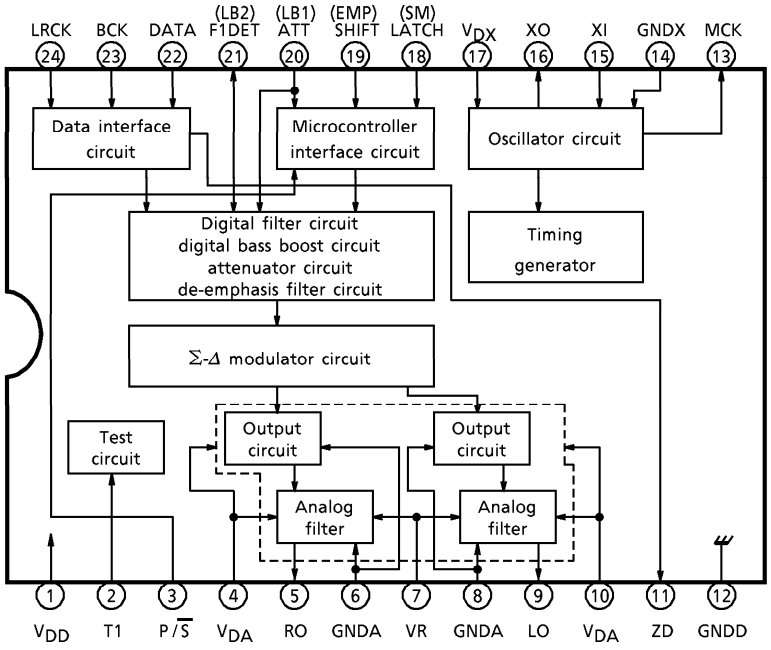
DA CONVERTER (V_{DD} = 5.0V)

	OSR	NOISE DISTORTION	S/N RATIO
Standard Operation	192fs	−85dB (Typ.)	96dB (Typ.)

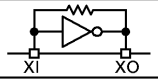
PIN CONNECTION



BLOCK DIAGRAM



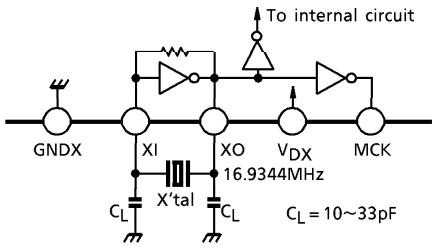
PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTION	REMARKS
1	V_{DD}	—	Digital block power supply pin.	
2	T1	I	Test pin. Always set at to "Low".	
3	P/$\overline{S}$	I	Parallel/serial mode select pin.	
4	V_{DA}	—	Analog power supply pin.	
5	RO	O	Right channel analog signal output pin.	
6	GNDA	—	Analog GND pin.	
7	VR	—	Reference voltage pin.	
8	GNDA	—	Analog GND pin.	
9	LO	O	Left channel analog signal output pin.	
10	V_{DA}	—	Analog power supply pin.	
11	ZD	O	Zero data detection output pin common to left and right channels.	
12	GNDD	—	Digital GND pin	
13	MCK	O	System clock output pin.	
14	GNDX	—	Crystal oscillator GND pin.	
15	XI	I	Crystal oscillator connecting pins. Generate the clock required by the system.	
16	XO	O		
17	V_{DX}	—	Crystal oscillator power supply pin.	
18	LATCH (SM)	I	In serial mode, data latch signal input pin. In parallel mode, soft mute control pin.	Schmidt input
19	SHIFT (EMP)	I	In serial mode, shift clock input pin. In parallel mode, de-emphasis filter control pin.	Schmidt input
20	ATT (LB1)	I	In serial mode, data input pin. In parallel mode, dynamic bass boost mode control pin 1.	Schmidt input
21	F1DET (LB2)	I/O	In serial mode, FLAT1 mode detection output pin In parallel mode, dynamic bass boost mode control pin 2.	
22	DATA	I	Data input pin.	
23	BCK	I	Bit clock input pin.	
24	LRCK	I	LR clock input pin.	

DESCRIPTION OF BLOCK OPERATIONS

1. Crystal oscillator circuit and timing generator

The clock required for internal operations is generated by connecting a crystal and condensers as shown in the diagram below.
The IC will also operate when a system clock is input from an external source through the XI pin (pin 15). However, in this situation, due consideration must be given to the fact that waveform characteristics, such as jitter and rising / falling characteristics of the system clock, significantly affect the DA converter's noise distortion and the S / N ratio.



Use a crystal with a low CI value and favorable start-up characteristics.
Fig.1 Crystal oscillator circuit configuration

The timing generator generates the clocks and calculation process timing signals required for such functions as digital filtering and de-emphasis filtering.

2. Data input circuit

DATA and the LRCK are loaded to the LSI internal shift registers on the BCK signal rising edge. It is consequently necessary for the DATA and LRCK signals to be synchronized and input on the BCK signal falling edge as indicated in the timing example below. Also, as DATA has been designed so that the 16 bits before the change point of LRCK are regarded as valid data, the data must be input afterwards when the BCK is 48fs or 64fs, etc.

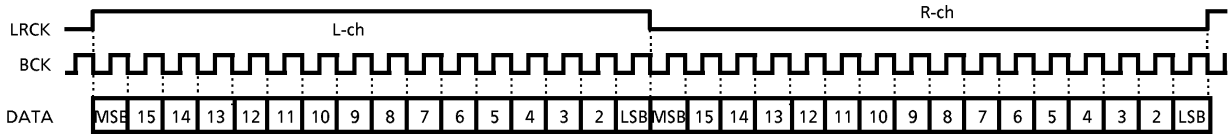


Fig.2a Input timing chart

When the BCK is 48fs or 64fs, the data is to be input afterwards as shown in the diagram below.

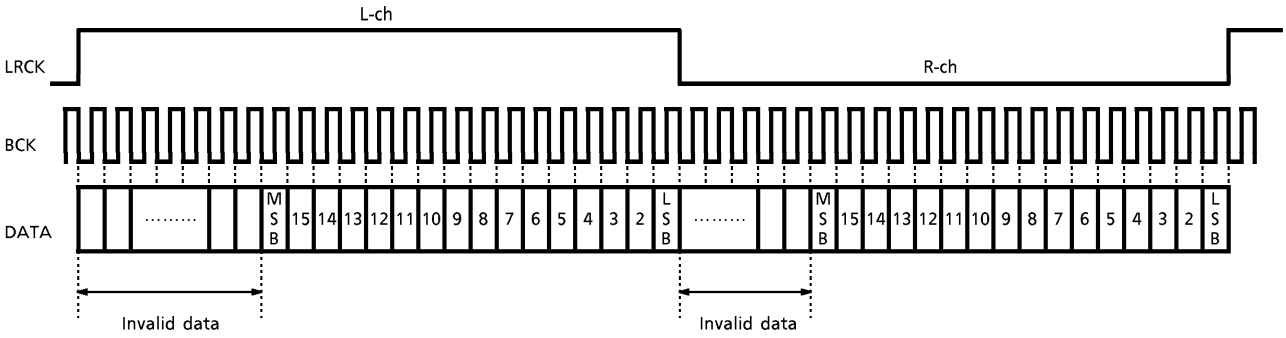


Fig.2b Example of Input timing chart

3. Digital filter

The 8-times oversampling IIR digital filter eliminates the noise returned from outside the bandwidth during standard operations.

Table-1. Basic characteristics of digital filter

SET MODE	PASSBAND RIPPLE	TRANSIENT BANDWIDTH	ATTENUATION
Standard Operations	±0.011dB	20.0k~24.1kHz	−26dB or less

The characteristics of the digital filter frequencies are shown below.

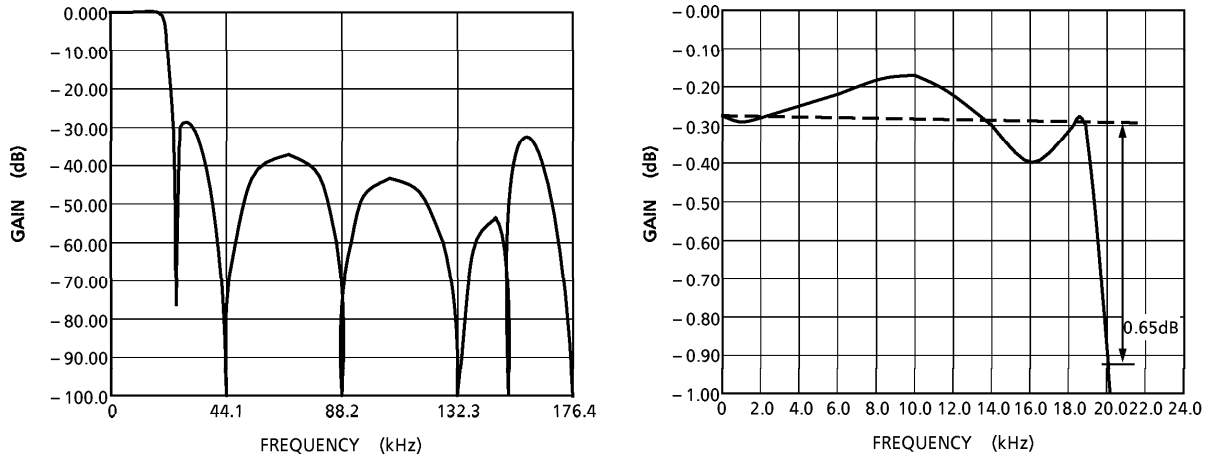


Fig.3 Digital filter frequency characteristics

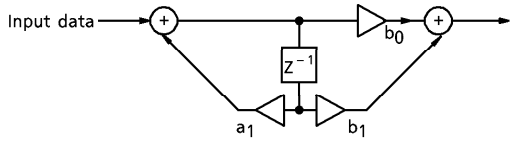
4. De-emphasis filter

ON / OFF is controlled in the parallel mode (P / $\overline{S}$ = "H") with the SHIFT (EMP) pin (pin 19).
This is set in the serial mode (P / $\overline{S}$ = "L") with a microcontroller or other equipment. (Refer to 11-2 Microcontroller setting mode for further details on serial mode settings.)

Table-2. De-emphasis filter settings (when in the parallel mode)

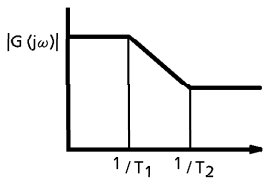
SHIFT (EMP) PIN	H	L
De-emphasis filter	ON	OFF

The digitalization of the de-emphasis filter eliminates the need for such external components as resistors, condensers and analog switches. In addition to this, the coefficients are aligned to reduce error in the de-emphasis filter characteristics.
The filter structure and characteristics are shown below.



Transfer function : $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Fig.4 IIR digital de-emphasis filter



$T_1 = 50\mu s$, $T_2 = 15\mu s$

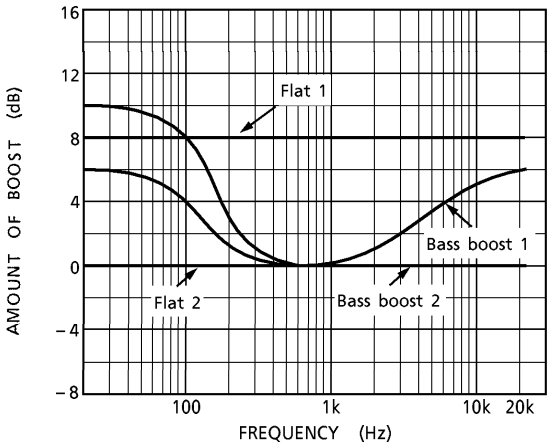
Fig.5 Filter characteristics

5. Digital bass boost circuit

It is possible to select between two types of bass boost with the following pin settings.

Table-3. Bus boost mode setting

LB1 (20 pin)	LB2 (21 pin)	Mode
L	L	Flat 2
L	H	Bass boost 1
H	L	Bass boost 2
H	H	Flat 1

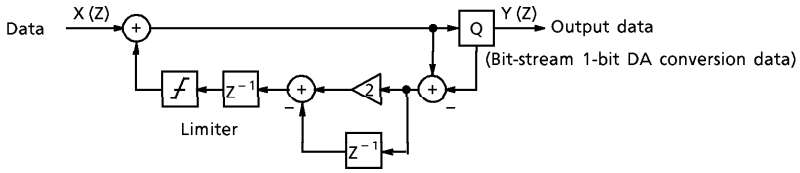


Note : Bass boost 2 matches with flat 2 when 1kHz or more

Fig.6 Bass boost characteristics

6. DA conversion circuit

The IC incorporates a second-order Σ-Δ modulation DA converter for two channels (simultaneous output type).
The internal structure of this is shown in fig.7.



Second-order Σ-Δ converter : $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Fig.7 Σ-Δ modulation DA converter structure

The Σ-Δ modulation clock has been designed to operate at 192fs.
The noise shaping characteristics are shown in fig.8.

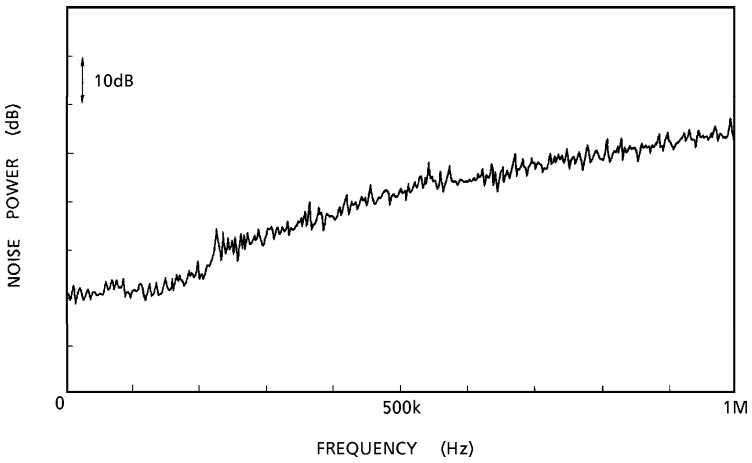


Fig.8 Noise shaping characteristics

7. Data output circuit

The output circuit is equipped with a third-order analog low-pass filter.
This enables direct analog signals to be acquired from the IC's RO (pin 5) and LO (pin 9) output pins.

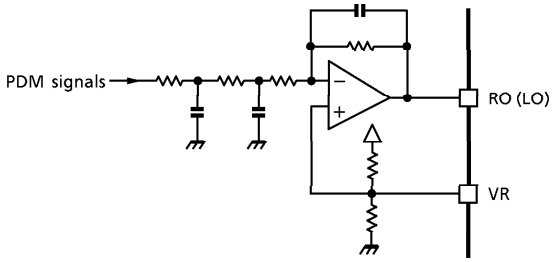


Fig.9 Analog filter circuit

8. Soft mute circuit

The IC is equipped with a soft mute function, and this enables a soft mute to be set for the DA converter output by switching the SM pin from the "L" level to the "H" level when in the parallel mode (P/$\overline{S}$ = "H"). The soft mute's ON/OFF function and the DA converter output are shown in fig.10.

The Soft mute ON/OFF control function is disabled during level transition.

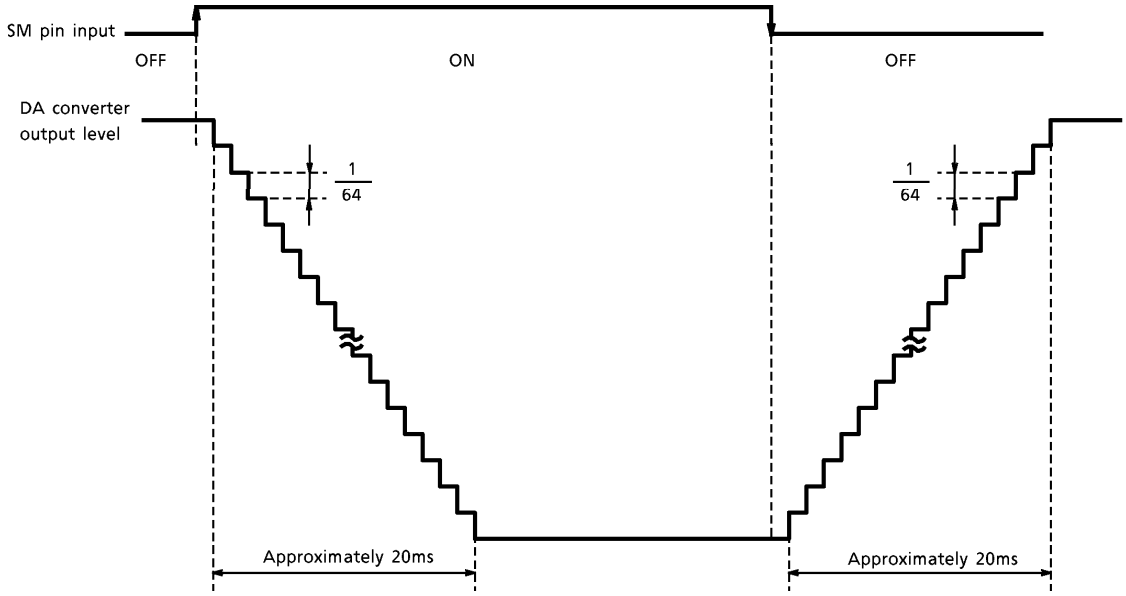


Fig.10 Changes in the soft mute DA converter output level

9. Zero data detection output circuit

The IC is equipped with a zero data detection output circuit, and pin ⑪ is switched from "L" to "H" when data for both the left channel and the right channel becomes zero data for approximately 350ms or longer.

This is fixed at "L" when the data for the left channel and right channel is not zero data.

10. FLAT1 mode detection output circuit

The IC is equipped with a FLAT1 mode detection function. The F1DET pin is switched from "H" to "L" when the FLAT1 mode is detected when in the serial mode (P/$\overline{S}$ = L).

This pin will remain at "H" when in any bus boost mode other than FLAT1.

11. Description of internal control signals

The P/$\overline{S}$ pin can be used to switch between the parallel control mode (P/$\overline{S}$ pin = "High" in DC setting mode) and the serial mode (P/$\overline{S}$ pin = "Low" with the microcontroller setting mode). The control settings are described below.

11-1 Parallel mode (P/$\overline{S}$ = "H" : DC setting mode)

Pins 18, 19, 20 and 21 are used as the mode setting pins shown in the table below when in the parallel mode.

Table-4. Pin names at the parallel mode

PIN No.	PIN NAME	PIN DESCRIPTION
18	SM	Soft mute control pin
19	EMP	De-emphasis control pin
20	LB1	Digital bass boost mode setting pin 1
21	LB2	Digital bass boost mode setting pin 2

11-2 Serial mode (P/$\overline{S}$ = "L" : Microcontroller setting mode)

It is possible to make the various settings with a microcontroller when in the serial mode. Pins 18, 19, 20 and 21 are used as the command input pins shown in the table below when in the serial mode.

Table-5. Pin names at the serial mode

PIN No.	PIN NAME	PIN DESCRIPTION
18	LATCH	Data latch signal input pin
19	SHIFT	Shift clock signal input pin
20	ATT	Data input pin
21	F1DET	FLAT1 mode detection output pin

The LATCH signals and ATT signals are loaded to the LSI internal shift registers on the SHIFT signal rising edge. It is consequently necessary for the data input from the ATT pin on the shift signal rising edge to be valid as indicated in the timing example in fig.11. It is also necessary for the LATCH pulse to rise at least 1.5μs after the final clock rising edge input from the SHIFT pin. Operating the shift clock with LATCH low destabilizes the internal state, which may lead to malfunctions, so it must therefore be set to the low level after loading D7 to the register.

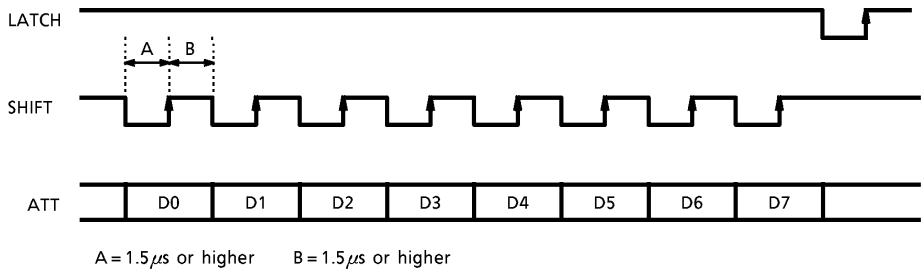


Fig.11 Example of Data setting timing in the serial mode

The various control settings when in the control mode are shown in the table below. Ensure that all control bits are set when the power supply is turned on.

Table-6. Serial mode control settings

SERIAL INPUT DATA	CONTROL SIGNALS	
	MODE 1	MODE 2
D7	0	1
D6	AT6	—
D5	AT5	μEMP
D4	AT4	μLB1
D3	AT3	μLB2
D2	AT2	MONO
D1	AT1	CHS
D0	AT0	—

AT0~6 : Attenuation level setting
μEMP : De-emphasis ON / OFF switch
μLB1 : Digital bass boost mode setting 1
μLB2 : Digital bass boost mode setting 2
MONO : Stereo / monaural setting
CHS : Output channel setting

11-2-1 Serial setting mode 1

Serial setting mode 1 is enabled when D7 = "L".

① Digital attenuator

The digital attenuation command is enabled when D7 = "L". The attenuation data can be set in 128 different ways. The relationship with the command's output is shown below.

Table-7. Attenuation data / audio data output

ATTENUATION DATA D6~D0	AUDIO OUTPUT
7F (HEX)	– 0.000dB
7E (HEX)	– 0.069dB
⋮	⋮
01 (HEX)	– 42.076dB
00 (HEX)	– ∞

01 (HEX) to 7E (HEX) : The attenuation value is obtained with the following equation.

$$ATT = 20\log (\text{input data} / 127)\ dB$$

Example : When the attenuation data is 7A

$$ATT = 20\log (122 / 127)\ dB = -0.349dB$$

11-2-2 Serial setting mode 2

Serial setting mode 2 is enabled when D7 = "H".

① Digital de-emphasis filter
Controlled with the μEMP and the μBS signals.

Table-8. Digital de-emphasis filter setting

μEMP	H	L
De-emphasis filter	ON	OFF

② Digital bass boost mode settings
Controlled with μLB1 and μLB2.

Table-9. Digital bass boost mode settings

μLB1	H	L	H	L
μLB2	H	H	L	L
Mode	Flat 1	Bass boost 1	Bass boost 2	Flat 2

When FLAT1 is selected in the serial mode, pin 21 will become the "L" level.

③ Stereo / monaural output channel settings
Set with MONO and CHS.

Table-10. Stereo, monaural and channel select settings

MONO	L	H	H
CHS	(*)	L	H
L, R-ch output	Stereo output	L-ch monaural output	R-ch output

(*) "H" or "L"

Note : The F1DET (LB2) pin (pin 21) will become the output pin in the serial mode and the input pin in the parallel mode.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~6.0	V
	V_{DA}	−0.3~6.0	
	V_{DX}	−0.3~6.0	
Input Voltage	V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta = 25°C, $V_{DD} = V_{DX} = V_{DA} = 5.0V$)

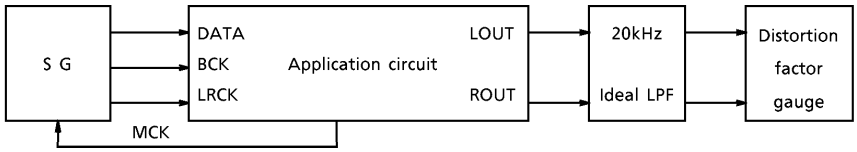
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Power Supply Voltage (1)		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Operating Power Supply Voltage (2)		V_{DD}	—	Ta = −15~50°C	2.7	3.0	5.5	V
		V_{DX}			2.7	3.0	5.5	
		V_{DA}			2.7	3.0	5.5	
Current Consumption		I_{DD}	—	XI = 16.9MHz	—	12	20	mA
Input Voltage	"H" Level	V_{IH}	—		$V_{DD} \times 0.7$	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	$V_{DD} \times 0.3$	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC CHARACTERISTICS (Oversampling Ratio = 192fs)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST	MIN	TYP.	MAX	UNIT
Noise Distortion 1	THD + N1	1	1kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5.0V$	—	−85	−80	dB
Noise Distortion 2	THD + N2	1	1kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0V$	—	−85	−78	dB
S / N Ratio	S / N	1		88	96	—	dB
Dynamic Range	DR	1	1kHz sine wave, −60dB input conversion	90	95	—	dB
Crosstalk	CT	1	1kHz sine wave, full-scale input	—	−95	−90	dB
Analog Output Level 1	Aout 1	1	1kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5.0V$	—	1150	—	mV_{rms}
Analog Output Level 2	Aout 2	1	1kHz sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0V$	—	700	—	mV_{rms}
Operating Frequency	f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 4.5V$	16.1	16.9344	17.8	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	41.9	44.1	46.3	kHz
	f_{BCK}		BCK duty cycle = 50%	1.34	2.1168	2.96	MHz
Rise Time	t_r	—	LRCK, BCK pins (10%~90%)	—	—	15	ns
Fall Time	t_f			—	—	15	
Delay Time	t_d	—	BCK ↓ edge → LRCK, DATA	—	—	40	ns

- **TEST CIRCUIT 1** : With the use of a sample application circuit

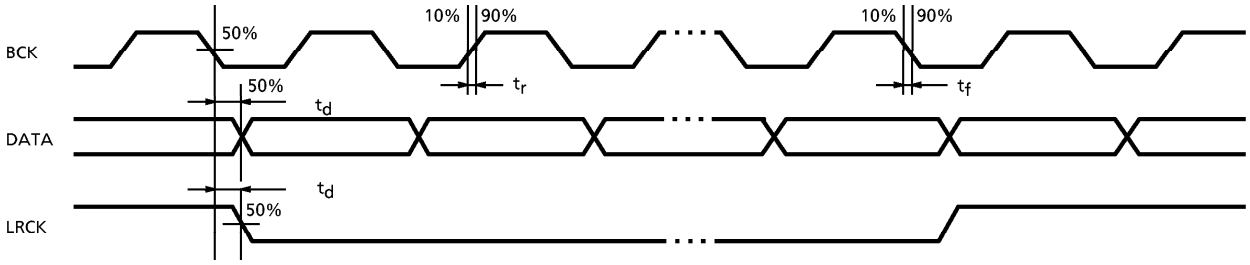


SG : Anritsu : MG-22A or equivalent
LPF : Shibasoku : Built-in 725C distortion factor gauge filter
Distortion : Shibasoku : 725C or equivalent

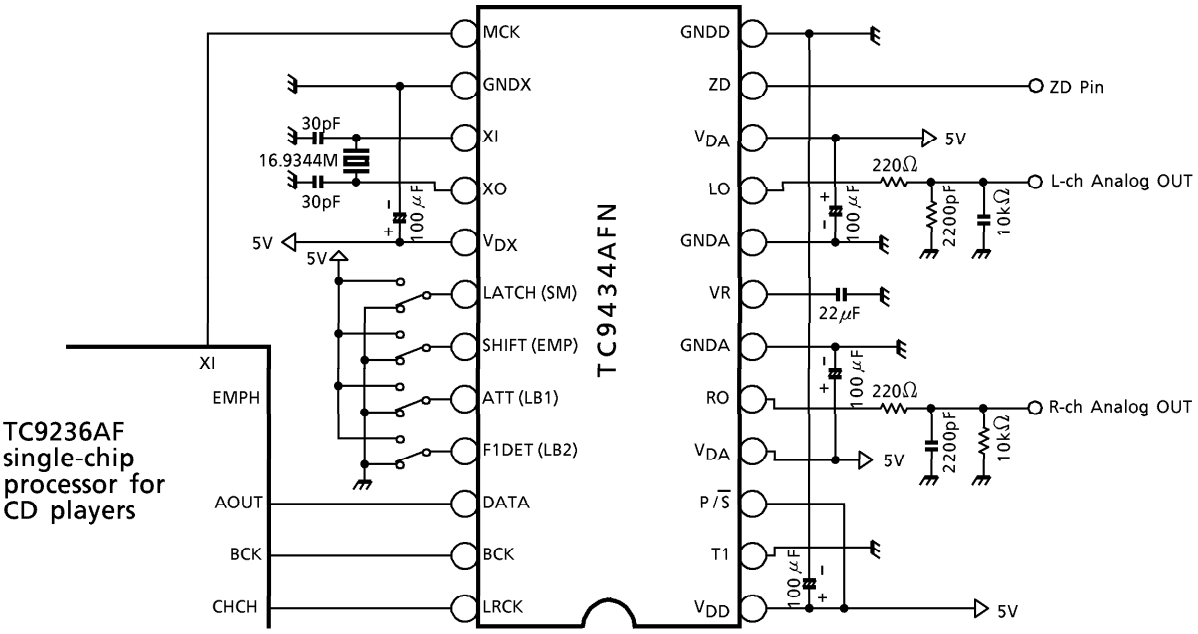
PARAMETER MEASURED	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S / N, DR	ON

A weight : IEC-A or equivalent

- **AC CHARACTERISTICS STIPULATED POINT** (INPUT SIGNAL STIPULATION : LRCK, BCK, DATA)



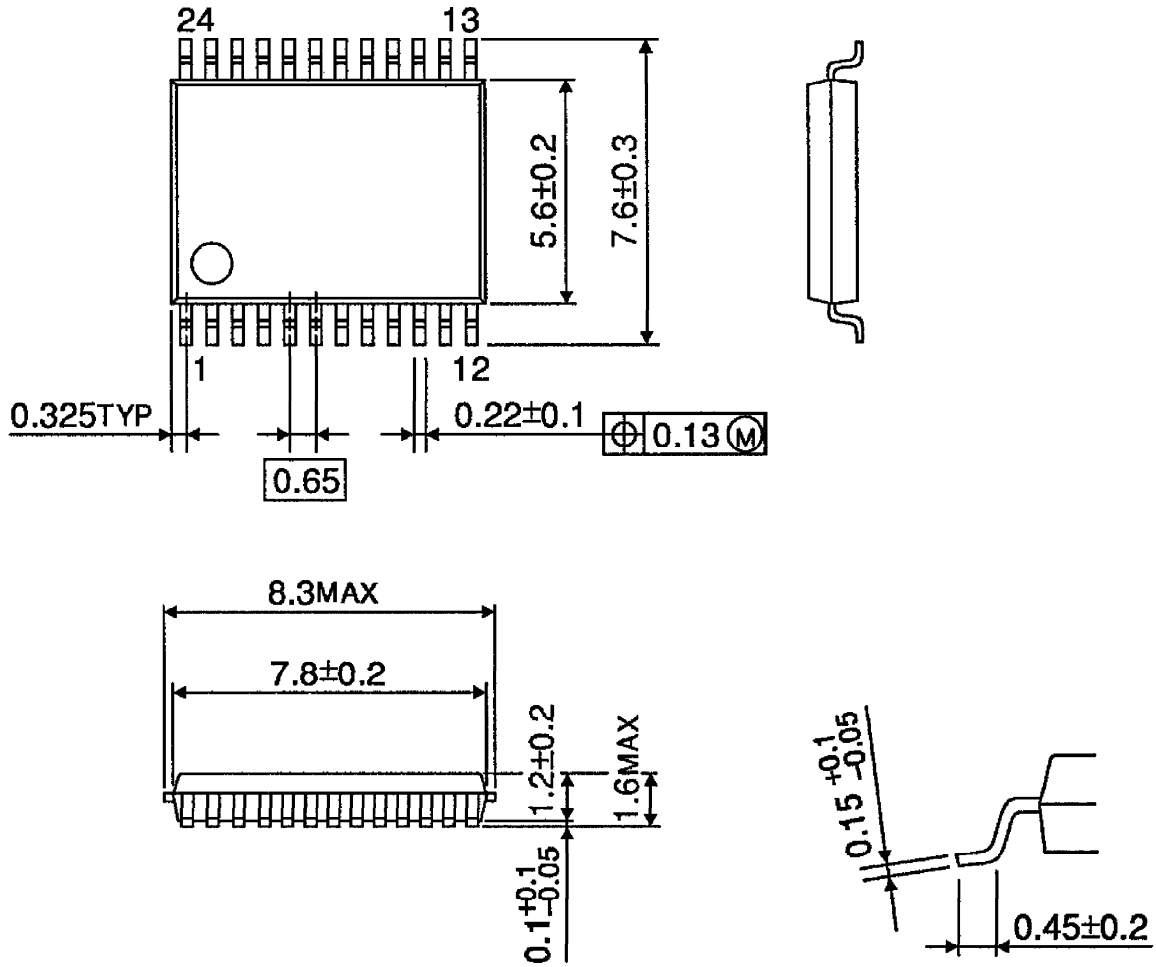
APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14g (Typ.)

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000707EBA

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