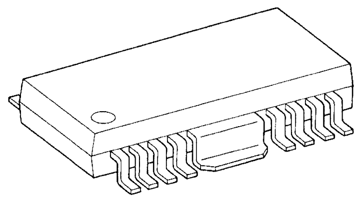
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8430AF

STEPPING MOTOR DRIVER IC

The TA8430AF is 2 Phase Bipolar Stepping Motor Driver IC designed especially for low operating voltage use FDD and other portable equipments.



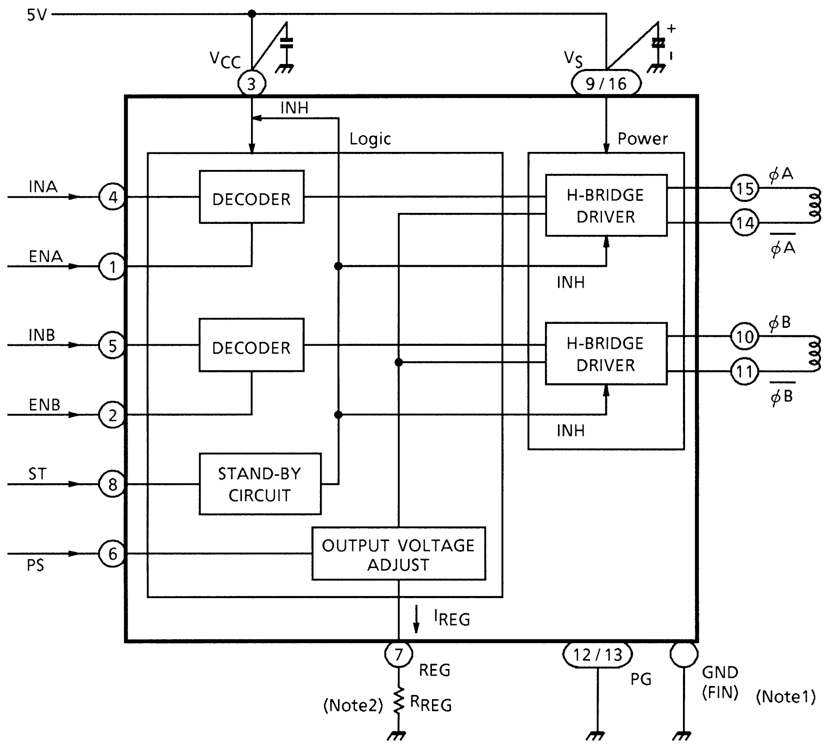
HSOP16-P-300-1.00

Weight : 0.50 g (Typ.)

FEATURES

- 2 Phase Bipolar Stepping Motor Driver
- Low Voltage Use : $V_{CC\ opr}$ = 4 V (Min.)
- Power Save and Stand−by Mode available
  I_{CC} stand−by ≤ 100 μA
- Built−in Punch Through Current Restriction Circuit
- 1, 2 and 1−2 Phase Excitation Drive available
- C−MOS Compatible Inputs (INA, INB, PS, ST)
- Output Current up to 400 mA (AVE) and 600 mA (PEAK)
- Sealed in PFP 16 SM Package
- HEAT SINK is connected with GND with low impedance.

BLOCK DIAGRAM



Note 1: GND terminal of 12 / 13 connect to FIN.

Note 2: Output Voltages, appeared at φA, $\overline{\varphi}$ A, φB and $\overline{\varphi}$ B, are adjusted by R_{reg} when Power Save function is selected.

Note 3: Utmost care is necessary in the design of the output line, V_{CC}, V_S and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

PIN FUNCTION

PIN No.	SYMBOL	FUNCTION
1	ENA	A channel enable
2	ENB	B channel enable
3	V_{CC}	Supply voltage
4	INA	A channel reciprocal switching
5	INB	B channel reciprocal switching
6	PS	Energy−saving signal input
7	REG	Output voltage setting
8	ST	Stand−by signal input
9	V_S	Supply voltage
10	φB	B output
11	$\overline{\varphi B}$	$\overline{B}$ output
12	PG	Power supply GND connection
13	PG	Power supply GND connection
14	$\overline{\varphi A}$	$\overline{A}$ output
15	φA	A output
16	V_S	Supply voltage
Fin	GND	GND connection

FUNCTION

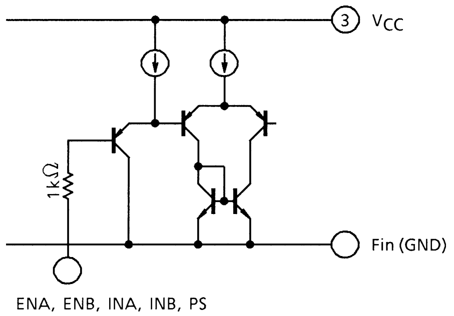
INPUT				OUTPUT		
ST	EN	PS	IN	φ	$\overline{\varphi}$	UPPER SIDE SATURATION VOLTAGE
H	H	L	L	L	H	$V_S - V_{CE}$ (SAT) U
H	H	L	H	H	L	$V_S - V_{CE}$ (SAT) U
H	H	H	L	L	H	V_{REG} (Note)
H	H	H	H	H	L	V_{REG} (Note)

Note: V_{REG} is a voltage appeared at PIN (7) and its value becomes approximately equal to V_{OUT} in power operation period.

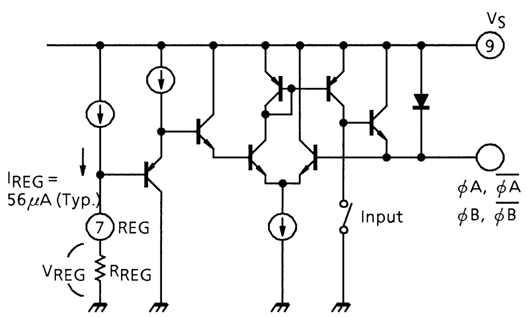
ST	ENA	ENB	φA, $\overline{\varphi A}$	φB, $\overline{\varphi B}$	MODE
H	L	H	∞	ENABLE	OPERATION
H	H	L	ENABLE	∞	OPERATION
H	H	H	ENABLE	ENABLE	OPERATION
L	X	X	∞	∞	STAND−BY

X: Don't Care
∞: High Impedance

INPUT STEP CIRCUIT DIAGRAM



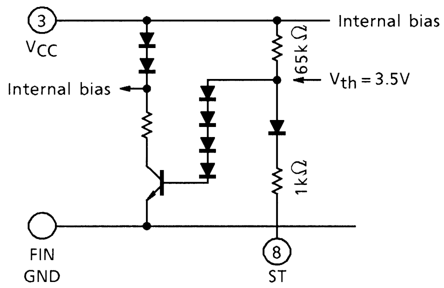
V_{REG} OUTPUT CIRCUIT DIAGRAM



V_{REG} output voltage can be selected with R_{REG} exterior resistance.
If V_{REG} is not used (as in the case of double−phase magnetization), use pin (7) in the open position.
(Do not connect to V_{CC} or GND pins.)
Use the following formula to obtain the output voltage.

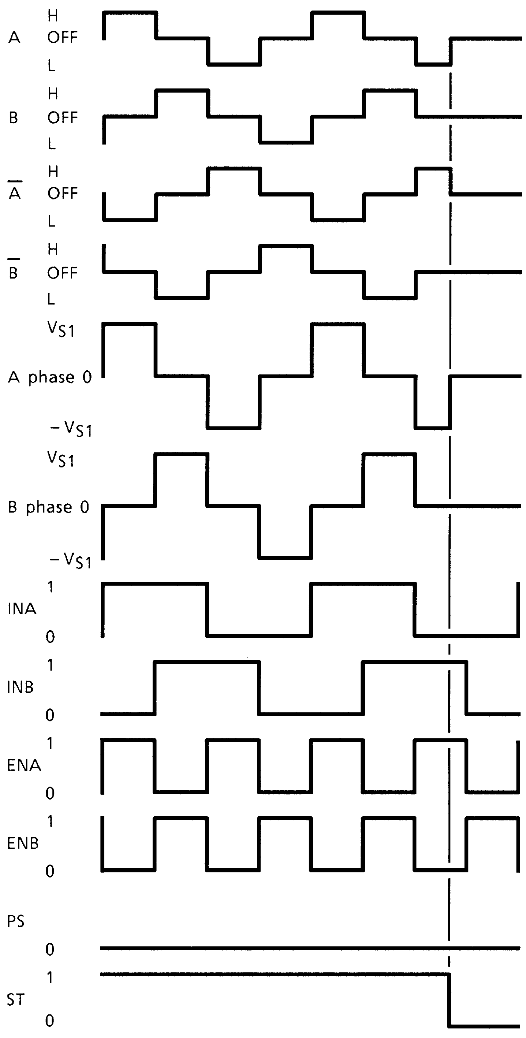
$$V_{OUT} \approx V_{REG} \approx R_{REG} \times 56 \times 10^{-6}$$

STAND−BY CIRCUIT DIAGRAM



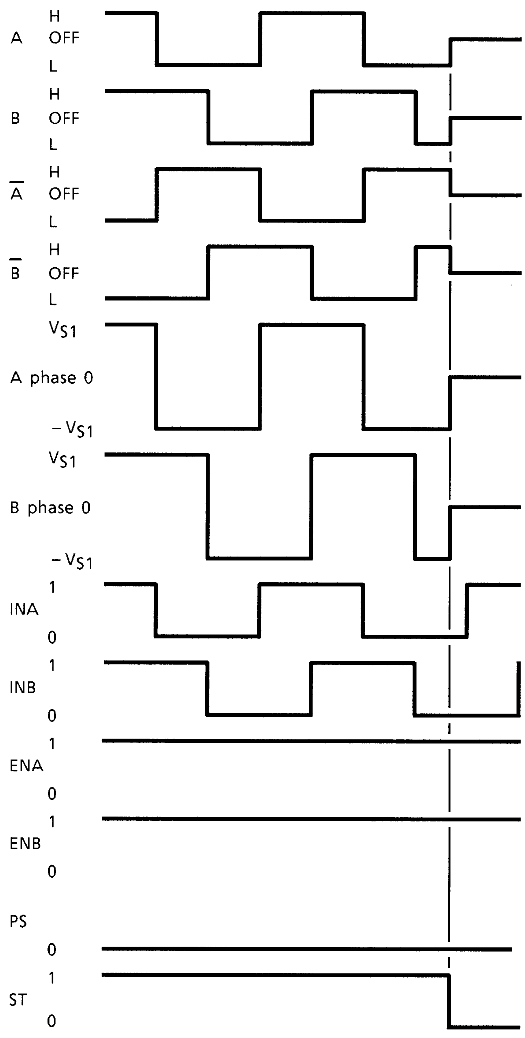
TIMING CHART

Single−phase magnetization



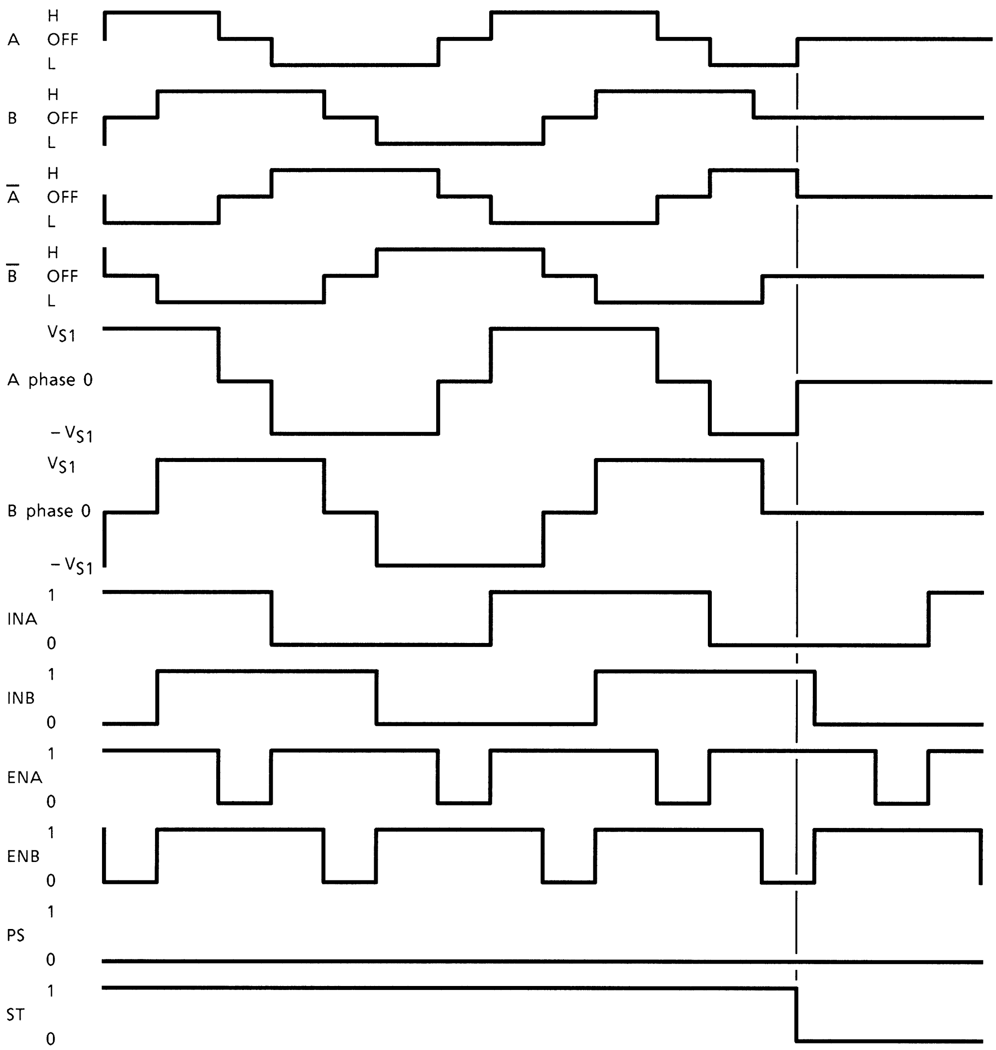
*: $V_{S1} = V_S - (V_{SAT\,U} + V_{SAT\,L})$

Double−phase magnetization



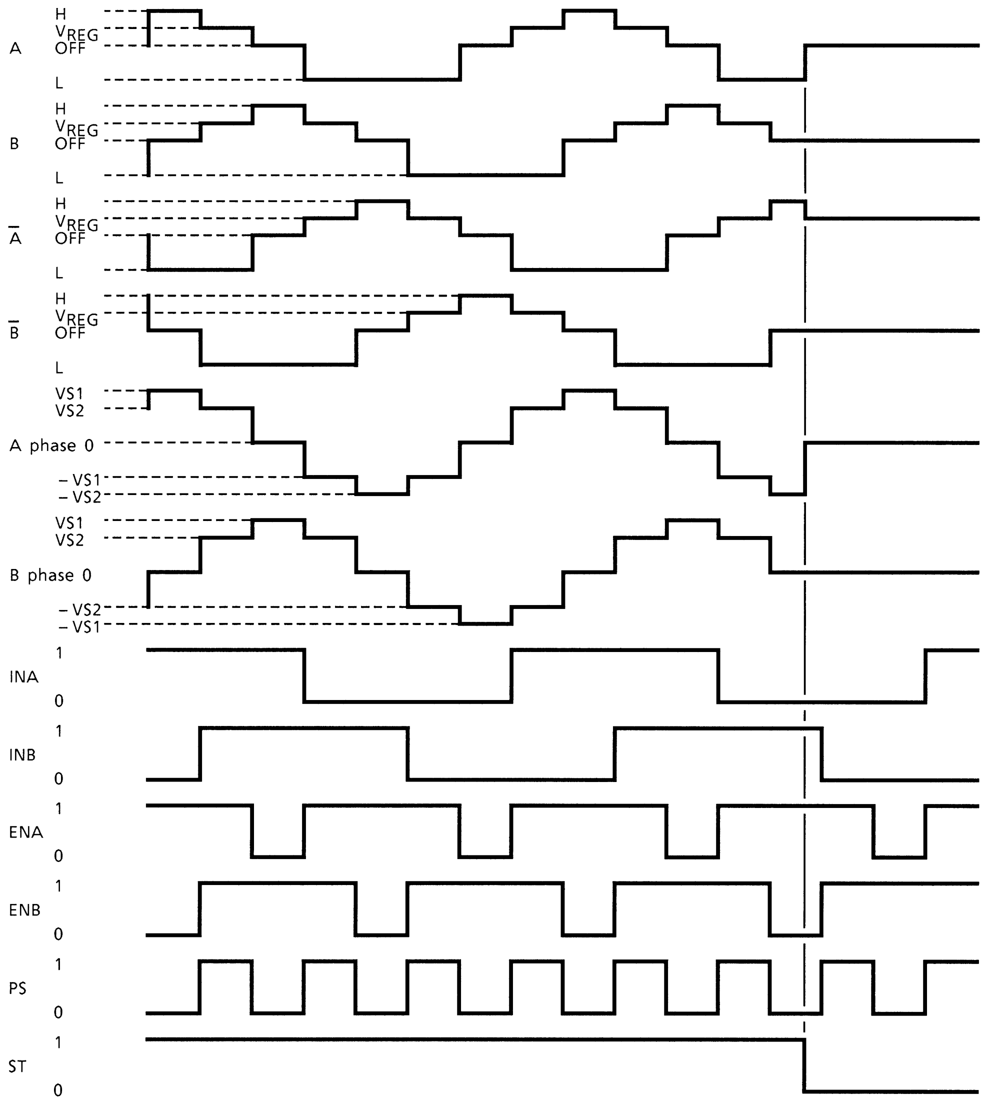
*: $V_{S1} = V_S - (V_{SAT\,U} + V_{SAT\,L})$

Single− / double−phase magnetization



*: $V_{S1} = V_S - (V_{SAT\,U} + V_{SAT\,L})$

Single− / double−phase magnetization (with energy−saving function)



$V_{S1} = V_S - (V_{SAT\,U} + V_{SAT\,L})$
$V_{S2} = V_{REG} - V_{SAT\,L}$

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	8.0	V
	V_S	8.0	
Output Current	$I_{O\ (MAX.)}$	±600	mA
	$I_{O\ (AVE.)}$	±400	
Input Voltage	V_{IN}, V_{PS} V_{ST}, V_{EN}	GND−0.4~V_{CC} + 0.4	V
Power Dissipation	P_D (Note)	1.4	W
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

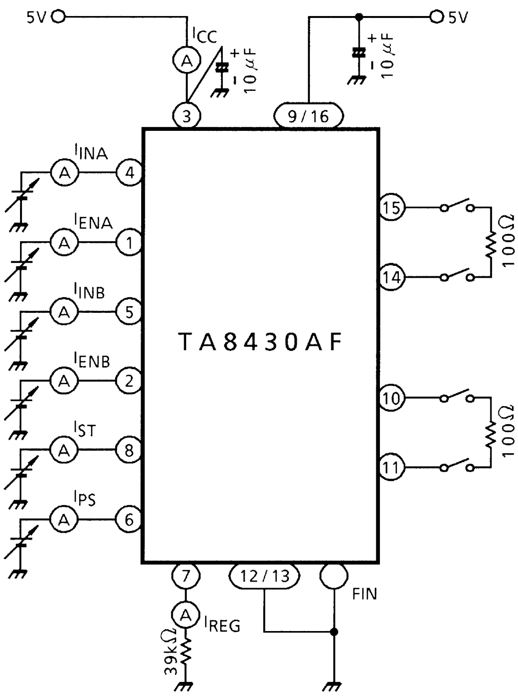
Note: 60 × 30 × 1.6 mm PCB occupied in excess of 50% of copper area, mounting.

ELECTRICAL CHARACTERISTICS
(Ta = 25°C, V_{CC} = 5 V, V_S = 5 V, ST = 5 V, PS = 0 V, EN = 5 V)

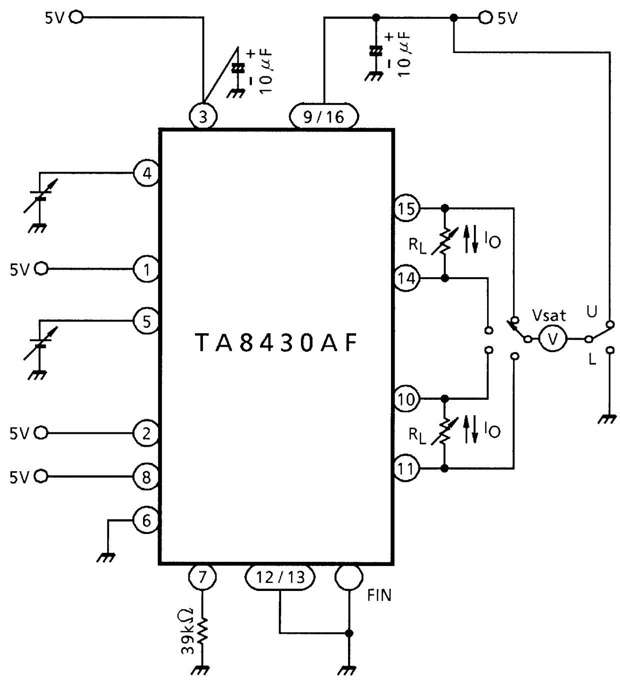
CHARACTERISTIC	SYMBOL	TEST CIR–CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Supply Current	I_{CC1}	1	Output open		—	14	20	mA
	I_{CC2}		Output open, PS = 5 V		—	14	20	
	I_{CC3}		Output open	ENA = 0 V, ENB = 5 V	—	9	15	
				ENA = 5 V, ENB = 0 V				
	I_{CC4}		Output open, PS = 5 V	ENA = 0 V, ENB = 5 V	—	9	15	
				ENA = 5 V, ENB = 0 V				
	I_{CC5}		ST = 0 V		20	65	110	μA
Input Voltage	V_{INH}	1	(4), (5) pin Source type		3.5	—	V_{CC}	V
	V_{INL}				GND	—	1.7	
	V_{ENH}, V_{PSH}		(1), (2), (6), (8) pin Source type		3.5	—	V_{CC}	
	V_{STH}							
	V_{ENL}, V_{PSL}				GND	—	1.7	
	V_{STL}							
Input Current	I_{INH}	1	V_{IN} = 3.5 V	(4), (5) pin	—	0	0.1	μA
	I_{INL}		V_{IN} = 0 V		—	0.25	5.0	
	I_{ENH}, I_{PSH}		V_{EN} = V_{PS} = 3.5 V	(1), (2), (6) pin	—	0	0.1	
	I_{ENL}, I_{PSL}		V_{EN} = $V_{P\ S}$= 0V		—	0.25	5.0	
	I_{STH}		V_{ST} = 3.5 V	(8) pin	—	0	0.1	
	I_{STL}		V_{ST} = 0 V		—	65	110	

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Saturation Voltage		$V_{SAT\ U1}$	2	—	I_{OUT} = 100 mA	—	0.8	—	V
		$V_{SAT\ U2}$			I_{OUT} = 400 mA	—	0.9	1.2	
		$V_{SAT\ L1}$			I_{OUT} = 100 mA	—	0.1	—	
		$V_{SAT\ L2}$			I_{OUT} = 400 mA	—	0.2	0.4	
Output Control Upper Voltage		$V_{REG}1$	—	R_{REG} = 39 kΩ	I_{OUT} = 100 mA	—	2.0	—	V
		$V_{REG}2$			I_{OUT} = 400 mA	—	1.9	—	
Control Circuit Output Current		I_{REG}	1	—		41	56	71	μA
Diode Forward Voltage		V_{FU}	3	IF = 400 mA		—	1.5	2.0	V
		V_{FL}				—	1.0	2.0	
Operating Supply Voltage Range		$V_{CC\ (opr.)}$	—	—		4.0	—	6.0	V
Propagation Delay Time	IN−φ	t_{pLH}	—	R_L = 8.2 Ω C_L = 15 pF		—	4.5	—	μs
	EN−φ					—	3	—	
	PS−φ					—	4.5	—	
	ST−φ					—	10	—	
	IN−φ	t_{pHL}				—	0.1	—	
	EN−φ					—	10	—	
	PS−φ					—	0.2	—	
	ST−φ					—	5	—	

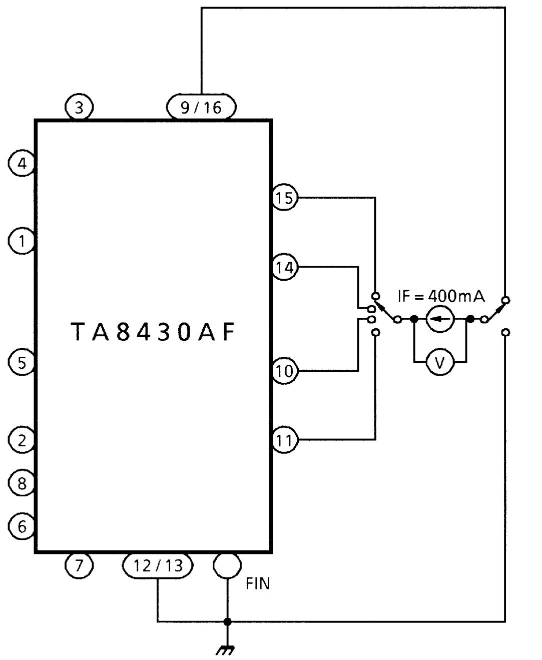
TEST CIRCUIT 1

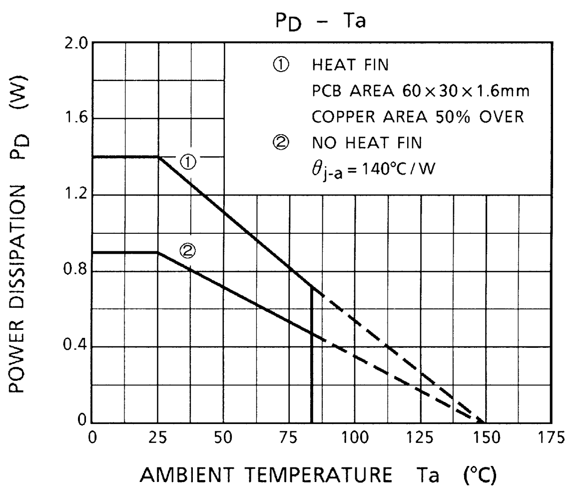


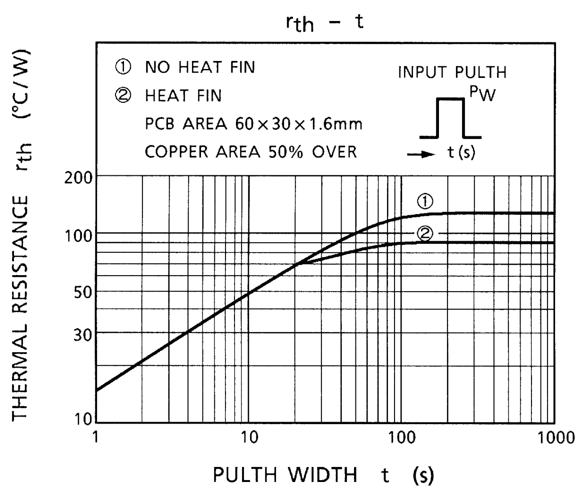
TEST CIRCUIT 2



TEST CIRCUIT 3

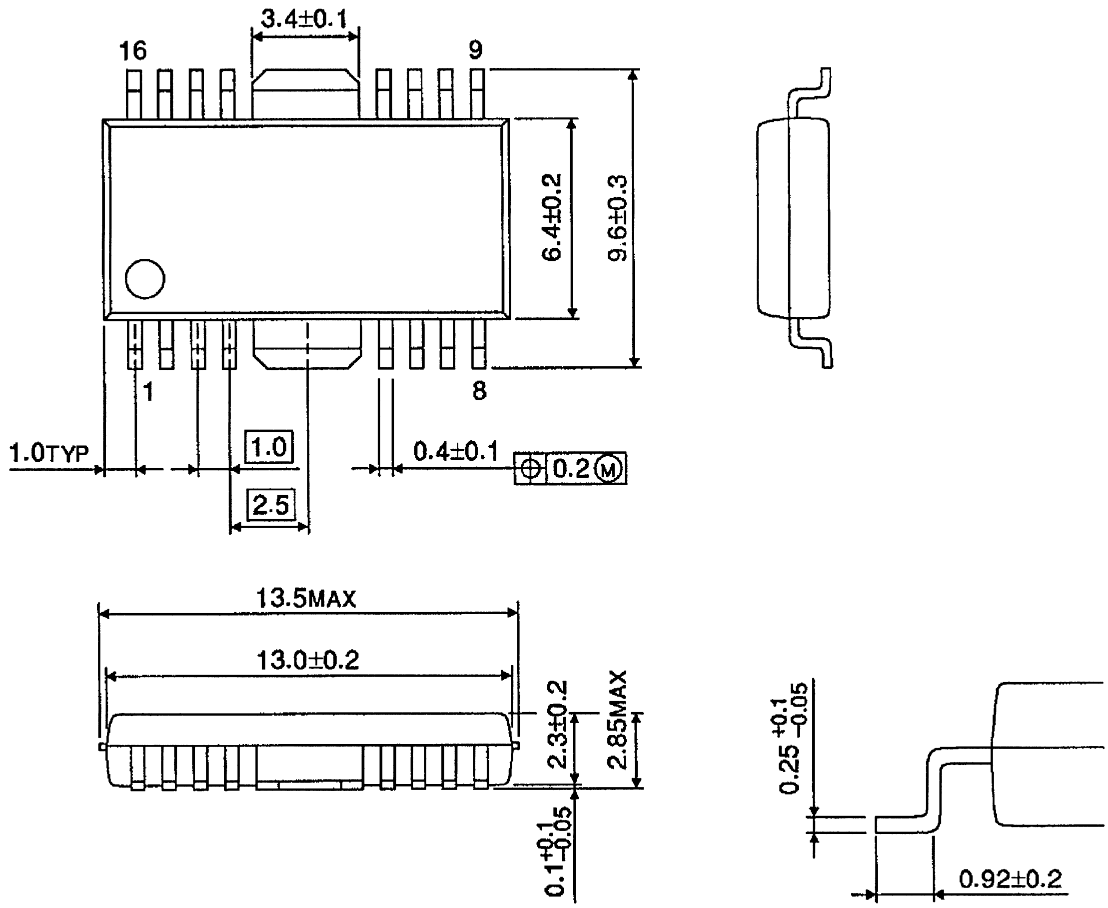






PACKAGE DIMENSIONS

HSOP16−P−300−1.00 Unit : mm



Weight : 0.50 g (Typ.)

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