Channelized T3 Termination with DS3 Framer, M13 Multiplexer, T1/E1 Framers and 256 Channel HDLC/PPP Controller

The TE3-CHATT is a serial communication controller which multiplexes up to 256 channels into a channelized DS3 trunk.

The unique integration of T1/E1 framer, M13 Multiplexer and DS2/DS3 framer reduces the layout complexity, saves cost and board space. This makes the TE3-CHATT an optimized solution for line cards at DS3 and higher bit rates, where access to DSO/DS1 channels is needed. Infineon's DS3 line interface unit, TE3-LIU (PEB 3452), completes your linecard.

Market's lowest PCI bus load enables multiple devices on the PCI bus, and maximizes the system throughput.



Applications

Channelized DS3 line cards at DS3 and higher bit rates

- Midrange Router
- Switches
- DSUs, CSUs, FRADs

General Features

- Supports a channelized DS3 link with a data rate of 45 MHz
- DS3 framer supports C-bit parity format and M13 asynchronous format
- M13 Multiplexer that maps 28 T1 signals or 21 E1 signals (ITU-T G.747) into a channelized DS3 signal
- 28 T1/21 E1 framer and signaling controller
- Direct connection to DS3 line interface unit or STS-1 mapper
- 256 bidirectional channels can be assigned arbitrarely to 28 links for HDLC, PPP or transparent processing

- Supports DS0, fractional T1/E1 or T1/E1 channels
- Provides remote line loads on DS1, DS2 and DS3 level
- Bit error rate tester can generate programmable pseudorandom test patterns
- Master/slave µP interface controls the layer one functions
- On-chip mailbox for communication between PCI subsystem and local processor
- The system interface is PCI V2.2 32 Bit running at 66 MHz
- FIFOs for DS1 and DS3 datalinks

Framer Aligner Features

- ITU-T G. 704 frame alignment/ synthesis for 2.048/1.544 kbit/s
- Detection of LOS (Red) Alarm, Insertion & Extraction of Alarms AIS, Remote (Yellow) Alarms
- Programmable frame formats: E1: Double- & CRC Multiframe T1: F4, SF (F12), ESF(F24)

Signaling Controller Features

- (F)DL-channel protocol for ESF ANSI T1.403 / AT&T TR54016
- Bit Oriented Messages (BOM)
- Time Slot 0 SA 8 4 bit handling via FIFOs

General

- JTAG boundary scan according to IEEE1149.1
- 0.25 μm, 2.5 V core technology
- I/Os are 3.3 V tolerant and have 3.3 V driving capability
- P-BGA-388 package
- Temperature range of -40 °C to +85 °C

Documentation and Support Package

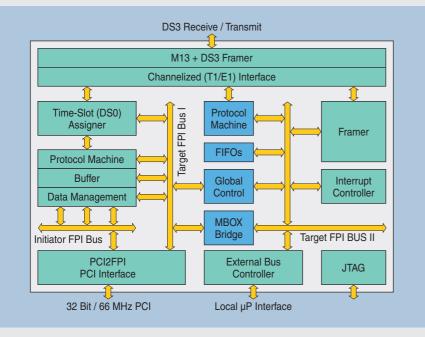
- Data Sheet
- Application Notes
- Evaluation System EASY256/3456
- DS3 Reference Design EASY3456-T3 with TE3-LIU (PEB 3452)

T E 3 - C H A T T P E B 3 4 5 6 E

www.infineon.com/t3



TE3-CHATT Block Diagram



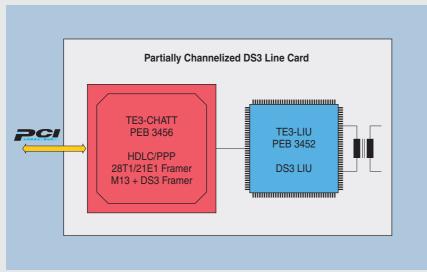
TE3-CHATT Evaluation Board



The EASY256/3456 is a PCI based evaluation board. Together with the low level software driver, this complete evaluation kit is speeding-up your development process.

The TE3-CHATT protocol machine handles HDLC, bit- and octet synchronous PPP and a transparent mode. Rate adoption for time slot transmission from 64 kbit/s down to 8 kbit/s and the concatenation of time slots, supporting the ISDN H0, H11, H12 channels is supported. Your software overhead is minimized due to the optimized descriptor structure well known from the MUNICH predecessors and the SCC product family. The integrated DS3 framer, M13 multiplexer and T1/E1 framer cover all important specifications and allow a direct connection to a DS3 line interface unit.

TE3-CHATT Application Example



Infineon offers a complete channelized DS3 line card solution using the TE3-LIU PEB 3452 together with the TE3-CHATT (PEB 3456). Please ask for the referring reference design EASY3456-T3.

Availability

The TE3-CHATT device is available with complete documentation and support package. A dedicated engineering support team is there to assist you. Please contact your local Infineon office for further details.

How to reach us: http://www.infineon.com

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